A NEW DUAL DAMASCENE PROCESS FLOW FOR POROUS LOW-K MATERIALS

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and more specifically to methods of dual damascene patterning.

BACKGROUND OF THE INVENTION

For porous low-k dielectric materials, traditional dual damascene patterning processes normally suffer surface roughness issues which will induce metallization issues. The major contribution to this surface roughness derives from the liner removal process (LRM). A trade-off between a sufficient LRM etch rate to open the stop layer and the dual damascene porous low-k surface roughness is very difficult to resolve.

U.S. Patent No. 6,350,681 B1 to Chen et al. describes a dual damascene comprising an etch via and an etch trench.

U.S. Patent No. 6,291,887 B1 to Wang et al. describes a dual damascene with low-k layers comprising an etch via and an etch trench with a nitride middle etch stop layer.

U.S. Patent No. 6,287,955 B1 to Wang et al. describes a dual damascene with multiple low-k intermetal dielectric layers comprising an etch via and an etch trench.

U.S. Patent No. 6,300,235 B1 to Feldner et al. describes a dual damascene with low-k layers comprising an etch via and an etch trench with sacrificial flowable oxide.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide a method of patterning dual damascene openings.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having an overlying exposed conductive layer formed thereover is provided. A dielectric layer is formed over the exposed conductive layer. An anti-reflective coating layer is formed over the dielectric layer. The anti-reflective layer and the dielectric layer are etched using a via opening process to form an initial via exposing a portion of the conductive layer. A protective film portion is formed over at least the exposed portion of the conductive layer. The anti-reflective coating layer and the dielectric layer are patterned to reduce the initial via to a reduced via and to form a trench opening substantially centered over the reduced via. The trench opening and the reduced via comprising the dual damascene opening.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 7 schematically illustrates a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

For the purposes of this invention, "low-k" means a dielectric constant of less than about 3.0.

Initial Structure - Fig. 1

As shown in Fig. 1, structure 10 includes an uppermost metal layer 12 formed thereover to a thickness of preferably from about 3000 to 15,000Å and more preferably from about 3000 to 8000Å.

Structure 10 is preferably includes a silicon or germanium substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

Metal layer 12 is preferably comprised of copper, aluminum, gold or silver and is more preferably copper.

An optional etch stop/liner layer 14 is formed over metal layer 12 to a thickness of preferably from about 50 to 2000Å and more preferably from about

100 to 1000Å. Etch stop/liner layer 14 is preferably comprised of the elements Si, O, N and/or C and may be specifically comprised of, for example, Si_3N_4, SiOCN, SiOC and SiC.

Porous low-k dielectric layer 16 is formed over optional etch stop/liner layer 14 to a thickness of preferably from about 2000 to 20,000Å and more preferably from about 2000 to 15,000Å. Porous low-k dielectric layer 16 has a dielectric constant (k) of preferably less than about 3.0, more preferably from about 1.0 to less than about 3.0 and most preferably from about 1.5 to 2.8 and is preferably comprised of the elements Si, O, C and/or H such as SiOCH.

An anti-reflective coating (ARC) layer 18 may be formed over porous low-k layer 16 to a thickness of preferably from about 50 to 2000Å and more preferably from about 100 to 1500Å. ARC layer 18 is preferably comprised of SiON or SiOC and is more preferably SiON.

Via Opening Process To Form Initial Via 20 - Fig. 2

As shown in Fig. 2, a via opening process is utilized to etch through ARC layer 18 and porous low-k layer 16 to form initial via 20 exposing a portion 15 of etch stop/liner layer 14. The via opening process is preferably a dry etch process employing an F-based plasma and is conducted under the following conditions:

temperature: preferably from about 0 to 200°C and more preferably from about 0 to 100°C; pressure: preferably from about 5 to 300 mTorr and more preferably from about5 to 250 mTorr;

time: preferably from about 10 to 500 seconds and more preferably from about 20 to 300 seconds; and

plasma power: preferably from about 0 to 3000 W and more preferably from about 50 to 2500 W.

Since the via opening process is conducted at this point in the processing, there is no surface roughness of the patterned porous low-k dielectric layer 16' as the LRM processing does not affect any remaining horizontal surface of the patterned porous low-k dielectric layer 16'.

Via 20 is preferably from about 200 to 3500Å wide and is more preferably from about 800 to 2500Å wide.

Liner Removal Process (LRM): Removal Of Exposed Etch Stop/Liner Layer Portion 15 - Fig. 3

As shown in Fig. 3, the exposed portion 15 of etch stop/liner layer 14 is removed by a liner removal process (LRM) preferably using a dry etch process employing a F-based plasma or a physical bombardment process employing, for example, Ar, He or N_2, to expose a portion 11 of metal layer 12.

Deposition Of Protective Film Portions 22, 24 - Fig. 4

As shown in Fig. 4, a protective film is deposited over the structure of Fig. 3 to form protective film portions 22 over the patterned ARC layer 18' and a protective film portion 24 over the exposed portion 11 of metal layer 12.

Protective film portions 22, 24 are preferably comprised of an organic chemical vapor deposition (CVD) film including the elements C, O and H such as C_xH_y and specifically such as, for example, C_2H_4 or C_2H_6, as will be used for illustrative purposes hereafter, and protective film portion 24 is used to protect the otherwise exposed metal portion thereunder to prevent damage to the metal during subsequent processing.

Organic CVD film portion 24 is formed to a thickness of preferably from about 50 to 2000Å and more preferably 200 to 1500Å.

Formation Of Via Plug - Fig. 5

As shown in Fig. 5, a via plug 27 is formed within initial via 20 and is preferably comprised of the elements C, H and/or O and may be comprised of conventional resist or BARC materials. Via plug 27 provides protection during the subsequent opening of trench 28 (see below) and assists in the patterning of the photoresist layer 26 (better planarization) (see below).

Via plug 27 may be formed of a via plug material layer and then etched back (along with protective film portion 22 to expose portions 31 of patterned ARC layer 18' as shown in Fig. 5) to leave via plug 27 within initial via 20 as shown in Fig. 5.

Formation Of Patterned Masking Layer 26 - Fig. 5

As shown in Fig. 5, a patterned masking layer 26 is then formed over exposed portions 29 of patterned ARC layer 18' leaving portions 31 of patterned ARC layer 18' adjacent initial via opening 20 exposed.

Patterned masking layer 26 is preferably photoresist.

Formation Of Trench Opening 28 - Fig. 6

As shown in Fig. 6, using patterned masking layer 26 as a mask, the underlying exposed portions 31 of patterned ARC layer 18' adjacent initial via opening 20 and a portion of the underlying patterned porous low-k dielectric layer 16' are removed to form trench opening 28 within twice patterned porous low-k dielectric layer 16'' substantially centered over etched via 20'. Trench opening 28 and etched via 20' comprise dual damascene opening 30. Via plug 27 is at least partially consumed during the formation of trench opening 28 leaving a residual portion 27' of via plug 27 remains within etched via 20' as shown in Fig. 6.

Alternatively, all of via plug 27 is removed, leaving the protective film portion 24 over the otherwise exposed portion of metal layer 12.

Trench opening 28 is preferably formed using a dry etch process employing an F-based plasma.

Trench opening 28 has a width of preferably from about 5000Å to 100μm.

Removal Of Patterned Masking Layer 26, Remaining Portion Of Via Plug 27 And Organic CVD Film Portion 24

As shown in Fig. 7, patterned masking layer 26, any remaining portion 27' of via plug 27 and the organic CVD film portion 24 are removed, preferably by ashing, and the structure is cleaned as necessary to complete formation of the dual damascene opening 30 without surface roughness.

Further processing may then proceed. For example a dual damascene structure may be formed within dual damascene opening 30 comprised of a metal such as copper, aluminum, gold or silver.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.